Abstracts

HiperLAN 5.4 GHz low power CMOS synchronous oscillator (2001 [RFIC])

Y. Deval, J.-B. Begueret, A. Spataro, P. Fouillat, D. Belot and F. Badets. "HiperLAN 5.4 GHz low power CMOS synchronous oscillator (2001 [RFIC])." 2001 Radio Frequency Integrated Circuits (RFIC) Symposium 01. (2001 [RFIC]): 53-56.

A 5.4 GHz 0.25 /spl mu/m VLSI CMOS synchronous oscillator is proposed, which is designed to act as a local oscillator for HiperLAN systems. The design strategy is described, including the synchronization range optimization approach. A chip is presented, which provides a 150 MHz synchronization range and a -97 dBc/Hz phase noise at 10 kHz offset from the carrier, while only consuming 5 mA from a 2.5 V supply.

❑ Return to main document.